Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1Y**
2. **1A**
3. **1B**
4. **2Y**
5. **2A**
6. **2B**
7. **GND**
8. **3B**
9. **3A**
10. **3Y**
11. **4B**
12. **4A**
13. **4Y**
14. **VCC**

**.037”**

**.038”**

**13 12 11 10 9**

**2 3 4 5 6**

**8**

**7**

**14**

**1**

**LS02**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: LS02**

**APPROVED BY: DK DIE SIZE .037” X .038” DATE: 6/26/23**

**MFG: MOTOROLA THICKNESS .014” P/N: 54LS02**

**DG 10.1.2**

#### Rev B, 7/1